Amendments to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the above-identified application.

Listing of Claims:

1. (currently amended) A microinstruction sequencer, ~~including~~ comprising:

a microinstruction sequencer stack comprising an array of memory cells; and

~~control~~ microinstruction sequencing logic to, ~~-~~ determine if there are any microinstructions being issued which affect the microinstruction sequencer stack~~said microinstruction sequencer stack coupled to receive data and control values from one of a microinstruction sequencing logic and a microprocessor core unit~~.

2-3. (cancelled)

4. (original) The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to:

generate a value of a microinstruction address;

add an intermediary value to the value of the microinstruction address to yield an incremented value;

send a control value to the microinstruction sequencer stack, said control value to cause the incremented value to be pushed onto the microinstruction sequencer stack; and

push the incremented value onto the microinstruction sequencer stack.

5. (original) The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to:

send a control value to the microinstruction sequencer stack, said control value to:

cause the microinstruction sequencer stack to pop a value; and

send the popped value to a microinstruction address multiplexer.

6. (currently amended) The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to:

send a control value to the microinstruction sequencer stack, said control value to:

cause the microinstruction sequencer stack to pop a value; and

send the popped value to an immediate logic, said immediate logic to pass the value to the ~~microinstruction~~ microprocessor core unit.

7. (original) The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack, said control value to cause the microinstruction sequencer stack to push a value in an immediate field of a microinstruction onto the microinstruction sequencer stack.

8. (original) The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack, said control value to cause the microinstruction sequencer stack to return to a reset state.

9. (original) The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack, said control value to cause the microinstruction sequencer stack to pop a value and send the popped value to an immediate logic.

10. (original) The microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack, said control value to cause the microinstruction sequencer stack to send a value at the top of the microinstruction sequencer stack to an immediate logic.

11-12. (cancelled)

13. (currently amended) A microprocessor including a microinstruction sequencer comprising:

an array of memory cells dedicated to said microinstruction sequencer;

an address multiplexer coupled to said array of memory cells;

sequencing logic coupled to said address multiplexer and to said array of memory cells, wherein the sequencing logic includes logic to determine if there are any microinstructions being issued which affect the microinstruction sequencer stack; and

a microprocessor core unit coupled to said array of memory cells.

14. (original) The microinstruction sequencer of claim 13, wherein the microprocessor core unit is an execution unit.

15. (original) The microinstruction sequencer of claim 13, wherein the microprocessor core unit is a retire unit.

16-17. (cancelled)